Dynamic Engineers Inc.
2550 Gray Falls Dr., Suite#128, Houston, TX, 77077
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VCTCXO-2.5-3.2-LVCMOS-xMHz
LVCMOS Voltage Controlled Temperature Compensated Crystal Oscillator

Features and Benefits

Frequency Range from 10 MHz to 245 MHz
2.5 mm x 3.2 mm x 1.6mm compact SMD package
Up to ±0.5 ppm stability (depends on operating temperature)
LVCMOS output
2.5V or 3.3V supply
Integrated phase jitter performance of 1.5 pS RMS
Low power consumption

Typical Applications

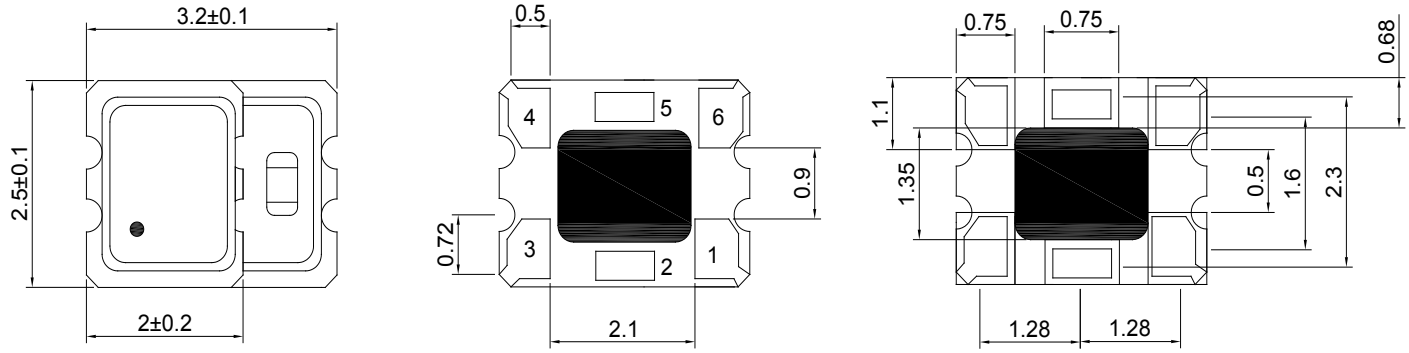
WiMAX, WLAN
Telecommunication
Mobile phone

Description

A new series of compact voltage controlled temperature compensated crystal oscillators with the latest low noise integrated circuit topologies.

Mechanical Drawing & Pin Connections

Drawing No:MD160046-1



Pin Connection

Pin	Funtion
1	Voltage Control
2	Output Enable
3	GND
4	Output
5	N.C.
6	Vcc

Unit : mm
1mm=0.0394inch

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Specifications

General Specifications at Ta = +25°C, CL = 15pF							
		Min.	Max.		Min.	Max.	
Supply Voltage V_{DD}		2.5V ±5%			3.3V ±5%		
Frequency Range		10MHz	245 MHz		10MHz	245 MHz	
Frequency Stability Vs. Temperature (ref to +25°C) Vs Voltage (±5%) input change Vs Load (±10%) condition change Vs Aging (per year at 25°C) Vs. Reflow (1 reflow and measured 24 hours afterwards)		±2.5 ppm over -30°C to +85°C (default) ±0.5 ppm over -30°C to +85°C (available) ±1.0 ppm over -40°C to +85°C (available) ±0.2 ppm max ±0.2 ppm max 1.0 ppm max 1.0 ppm max					
Current Consumption All values are typical and over the operating temperatures		V_{DD} = +2.5V 50 MHz : 24 mA 125 MHz : 28 mA 200 MHz : 30 mA			V_{DD} = +3.3V 50 MHz : 26 mA 125 MHz : 30 mA 200 MHz : 34 mA		
Current with Output Disabled		18 mA (typical)					
Load		15 pF					
Output Logic High "1" Low "0"		 90% V_{DD} 10% V_{DD}					
Rise Time / Fall Time		1.5 nS (typical), 3.0 nS (max) Tr / Tf : 10% ↔ 90% waveform					
Initial Calibration Tolerance		±1.0 ppm max. at +25°C ±2°C (at shipment)					
Phase Noise [dBc / Hz (typical)]	Offset	**77.76**	**156.25**	**212.5**	**622.08**	**1000**	**1250**
	10 Hz	-62	-65	-61	-51	-40	-43
	100 Hz	-100	-92	-90	-79	-73	-75
	1 KHz	-116	-108	-106	-97	-91	-889
	10 KHz	-122	-114	-110	-102	-99	-95
	100 KHz	-124	-117	-112	-103	-99	-96
	1 MHz	-144	-139	-133	-125	-121	-117
	10 MHz	-152	-147	-142	-134	-129	-127
Phase Jitter (12KHz ~ 20 MHz, RMS) unit : pS		0.9	0.9	1.2	1.1	1.1	1.2
Duty Cycle		50% ±5%					
Start-up Time		5m sec max.					
Aging at Ta = +25°C		± 2 ppm max. first year at 25°C ; ± 10 ppm max. over 10 years					
Storage Temperature		-55°C to +150°C					

Control Voltage Function on Pad 1		Output Enable Function on Pad 2	
Control Voltage Center and Range	+1.5V ±1.0V for both V_{DD} = 2.5V and 3.3V	**OE Control on Pad 2**	0.7 of V_{DD} (min.) or no connection to enable output. LVCMOS / LVTTL level.
Frequency Pulling Range	±8 ppm min.		0.3 of V_{DD} (max.) to disable output (high impedance). LVCMOS / LVTTL level
Linearity	±1% typical. ±10% max	**Output Enable Time / Disable Time**	200 nS. Max. / 50 nS. Max
Transfer Function	Positive Transfer	**Integrated Phase Jitter**	1.5 pS typical (12 KHz to 20 MHz)
Absolute Voltage	4.0V max.		<400 fS (1.875 KHz to 21 MHz)
Input Impedance	770KΩ typical		
Harmonics	-5.0 dBc max.		

Other customized specifications maybe available. Please contact Dynamic Engineers Inc. for further details.