Dynamic Engineers Inc.
2550 Gray Falls Dr., Suite#128, Houston, TX, 77077
TEL: 1-281-870-8822 EMAIL: Sales@DynamicEng.com

VCXO5300R-LVDS
LVDS 10 to 1450 MHz Voltage Controlled Oscillator

Features and Benefits

Frequency Range 10 MHz to 1450 MHz
5.0 mm x 3.2 mm 6 pads ceramic SMD package
±50 ppm total stability over -40°C to +85°C
LVDS outputs
3.3V supply
Integrated phase jitter of 1.0pS RMS

Typical Applications

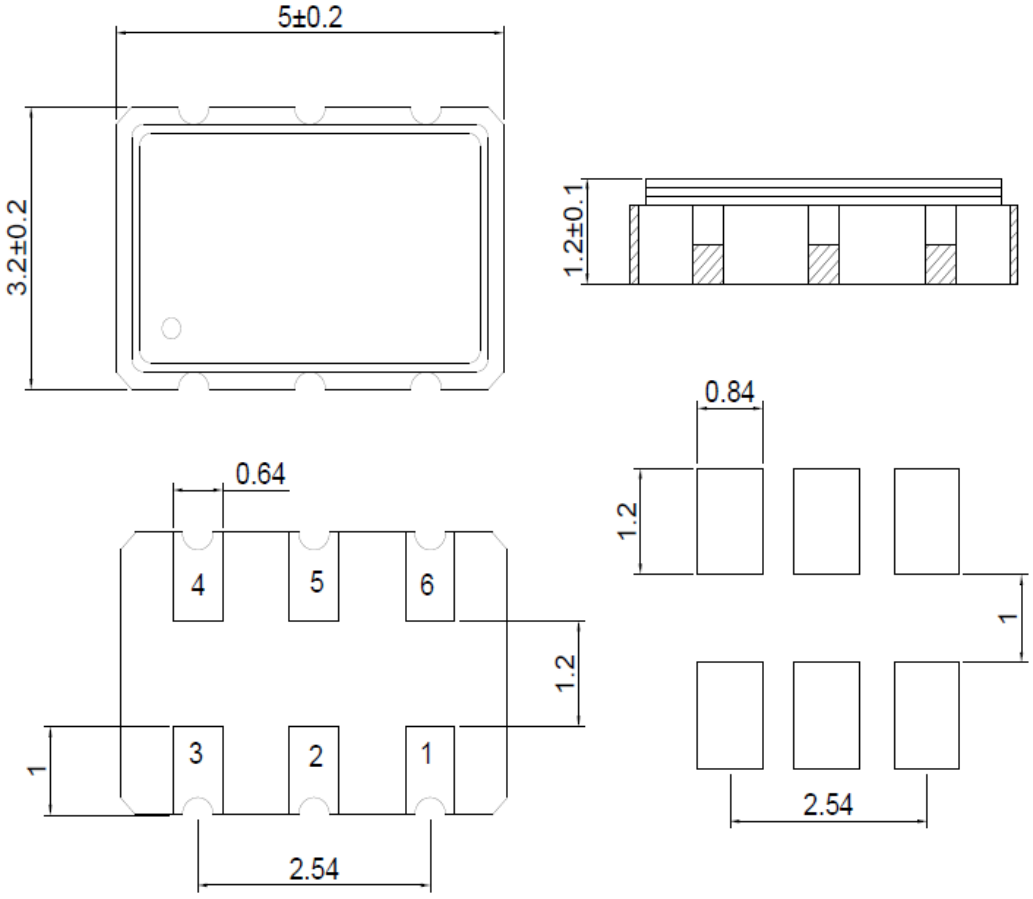
WiMax/WLAN
xDSL/VoIP, cable modem
Set-top Box, HDTV

Description

A new generation of voltage controlled oscillators with the latest tight symmetry topologies.

Mechanical Drawing & Pin Connections

Drawing No: **MD160040-1**



Pin Connection

Pad 1	Control Voltage
Pad 2	Tri-state
Pad 3	Ground
Pad 4	Differential
Pad 5	Complementary
Pad 6	Supply Voltage

Unit : mm
1mm=0.0394inch

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Specifications

General Specifications				
Output Logic Type		LVDS		
Parameter		3.3V		
		Min.	Typical	Max
Frequency Range		10MHz		1450MHz
Load		Differential		
Current Consumption (V_{DD} = +3.3V)		100MHz : 25mA		750MHz : 39mA
		250MHz: 30mA		1GHz : 43mA
		500MHz: 35mA		1.35GHz : 47mA
Output Level				
Output "High" Voltage; V_{OH}			1.4V	1.6V
Output "Low" Voltage; V_{OL}		0.9V	1.1V	
Current with Output		16mA typical		
Phase Noise		**125MHz**		**1000MHz**
	10Hz	-69dBc / Hz		-46dBc / Hz
	100Hz	-97dBc / Hz		-80dBc / Hz
	1 kHz	-114dBc / Hz		-96dBc / Hz
	10 kHz	-124dBc / Hz		-105dBc / Hz
	100KHz	-129dBc / Hz		-108dBc / Hz
	1MHz	-136dBc / Hz		-116dBc / Hz
	10MHz	-154dBc / Hz		-135dBc / Hz
Phase Jitter (12KHz ~ 20MHz, RMS)		0.5pS		0.7pS
Rise Time (Tr)/Fall Time (Tf) Tr/Tf: 20% – 80% waveform			0.2nS	0.4nS
Duty Cycle		50% ±5%		
Start-up Time				10ms max
Aging at Ta = +25°C First year at 25°C Over 10 years				±2 ppm ±10 ppm
Storage Temp. Range		-55°C to +150°C		
Control Voltage Function on Pad 1				
Supply Voltage (V_{DD})		VDD = +3.3V ; Vcon Center = +1.65V		
Vcontrol Range		+0.3V ~ +3.0V		
Frequency Pulling Range		±100ppm (min). Up to ±200ppm (min.) available		
Absolute Voltage		4.0V max. for 3.3V VDD		
Linearity		±5% typical. ±10% max.		
Input Impedance		1M Ω typical		
Bandwidth		10KHz min. measured at -3dB		
Transfer Function		Positive Transfer		

Output Enable Function		
OE Control on Pad 1	0.7 of VDD (min.) or no connection to enable output. 0.3 of VDD (max.) to disable output (high impedance)	
Output Enable Time / Disable Time	200 nS. Max / 50 nS. Max.	
Integrated Phase Jitter	0.6 pS typical (12 KHz to 20 MHz) ; <100 fS (1.875 KHz to 20 MHz)	
Stability vs. Temperature Range Availability		
	Temperature Range	
Stability in ppm	-10°C to +70°C	-40°C to +85°C
±100	Available	Available
±50	Available	Available

Other customized specifications may be available. Please contact Dynamic Engineers Inc. for further details.

Test Data

125 MHz LVDS Outputs

1000 MHz LVDS Output